WX1860 Datasheet

2023.6

Revision History

Revision	Data	Comments
0.1	2018.12	Initial revision
0.2	2019.8	Add DC characteristics and footprint
0.3	2019.9	Add ordering information
0.4	2019.10	Change Emerald to WX1860, update section 1.3.4
0.5	2019.11	Update pin description
0.6	2019.11	Add suggested SPI flash and MDI signal description
0.7	2019.12	Add IO DC specification
0.8	2020.7	Add single-port WX1860A1 and WX1860AL1
0.9	2020.12	Update clock input description
1.0	2021.1	Update duplex mode support
1.1	2021.11	Update order information
1.2	2023.6	Add SPI clock description

Table of Contents

1 Feature List

1.1 Network Feature

Feature	I350	WX1860
10/100/1000 Copper PHY integrated on-chip	4 ports	1/2/4 ports
Jumbo frames supported	9.5 KB	9.5 KB
Flow control support: send/receive PAUSE frames and receive FIFO thresholds	Y	Y
Statistics for management and RMON	Y	Y
802.1q VLAN support	Y	Y
802.3az EEE support	Y	Y
MDI Flip	Y	Y
SerDes interface for external PHY connection or system interconnect	4 ports	N
1000BASE-KX interface for Blade Server Backplane connections	Y	N
802.3ap Backplane Auto-negotiation	N	N
SGMII interface for external 1000BASE-T PHY connection	4 ports	N
RGMII interface for external PHY	N	1/2/4 ports
Fiber/copper auto-sense	4 ports	N
SerDes support of non-Auto-Negotiation partner	Y	N
SerDes signal detect	Y	N
External PHY control I/F MDC/MDIO	shared or perfunction	perfunction

Feature	I350	WX1860
External PHY control I/F 2 wire I/F	perfunction	perfunction
IPsec with SM4-GCM algorithm	N	Y
LinkSec with SM4-GCM algorithm	N	Y
Duplex mode support	Full/Half duplex	Full duplex

1.2 PCIe Feature

Feature	I350	WX1860
Max Link Speed	Gen2x4	Gen2x4
Max Payload Size	512 B	128 B
Max Read Request Size	2 KB	128 B
VPD	Y	Y
ECRC	Y	Y
LTR	Y	N
CSR access via Configuration space	Y	N
ACS	Y	N
AER	Y	Y
Multiple PF	4	4
DCA support	Y	N
TPH support	N	Y
PF FLR	Y	Y
SR-IOV	8VF/PF	8VF/PF

Feature	I350	WX1860
VF AER	Y	Y
VF FLR	Y	Y
64-bit BAR	Y	Y
MSI	Y	Y
MSI-X	32/PF	32/PF
VF MSI-X	2/VF	2/VF

1.3 LAN Feature

Feature	I350	WX1860
Programmable host memory receive buffers	Y	Y
Descriptor ring management hardware for transmit and receive	Y	Y
Software controlled global reset bit (resets everything except the configuration registers)	Y	Y
Software Definable Pins (SDP) - per port	4	4
Four SDP pins can be configured as general purpose interrupts	Y	Y
Wake up	Y	Y
Flexible wake-up filters	8	8
Flexible filters for queue assignment in normal operation	8	N
IPv6 wake-up filters	Y	Y
Default configuration by the EEPROM for all LEDs for pre-driver functionality	4 LED	4 LED
LAN function disable capability	Y	Y

Feature	I350	WX1860
Programmable memory transmit buffers	Y	Y
Double VLAN	Y	Y
IEEE 1588	Y	Y
Per-Packet Timestamp	Y	N
TX rate limiting per queue	N	N
TCP segmentation offload Up to 256 KB	Y	Y
iSCSI TCP segmentation offload (CRC)	N	N
IPv6 support for IP/TCP and IP/UDP receive checksum offload	Y	Y
Fragmented UDP checksum offload for packet reassembly	Y	Y
Message Signaled Interrupts (MSI)	Y	Y
Message Signaled Interrupts (MSI-X) number of vectors	25	36
Packet interrupt coalescing timers (packet timers) and absolute delay interrupt timers for both transmit and receive operation	Y	Y
Interrupt throttling control to limit maximum interrupt rate and improve CPU utilization	Y	Y
Rx packet split header	Y	Y
Receive Side Scaling (RSS) number of queues per port	up to 8	up to 8
Total number of Rx queues per port	8	8
Total number of TX queues per port	8	8
RX header replication	Y	N
Low latency interrupt	Y	Y
TCP timer interrupts	Y	Y

Feature	I350	WX1860
No snoop	Y	Y
Relax ordering	Y	Y
TSO interleaving for reduced latency	Y	Y

1.4 Virtualization Features

Feature	I350	WX1860
Support for Virtual Machines Device queues (VMDq) per port	8 pools single queue	8 pools single queue
L2 MAC address filters (unicast and multicast)	32	32
L2 VLAN filters	per pool	per pool
PCI-SIG SR-IOV	8 VF	8 VF
Multicast/Broadcast Packet replication	Y	Y
VM to VM Packet forwarding (Packet Loopback)	Y	Y
MAC and VLAN anti-spoofing	Y	Y
Per-pool statistics	Y	Y
Per-pool off loads	Y	Y
Per-pool jumbo support	Y	Y
Mirroring rules	4	4
External switch VEPA support	Y	Y
Promiscuous modes	VLAN, unicast, multicast	VLAN, unicast, multicast
ETAG	N	Y

1.5 Management Feature

Feature	I350	WX1860
Advanced pass-through-compatible management packet transmit/receive support	Y	Y
Managed ports on SMBus interface to external BMC	4	4
Auto-ARP reply over SMBus	Y	Y
NC-SI Interface to an External BMC	Y	Y
Standard DMTF NC-SI protocol support	Y	Y
DMTF MCTP protocol over SMBus	Y	Y
NC-SI HW arbitration	Y	N
OS to BMC traffic	Y	Y
L2 address filters	2	4
VLAN L2 filters	8	8
EtherType filters	4	4
Flex L4 port filters	8	16
Flex TCO filters	1	4
L3 address filters (IPv4)	4	4
L3 address filters (IPv6)	4	4
Build-in Temperature sensor	N	Y

1.6 Algorithm Feature

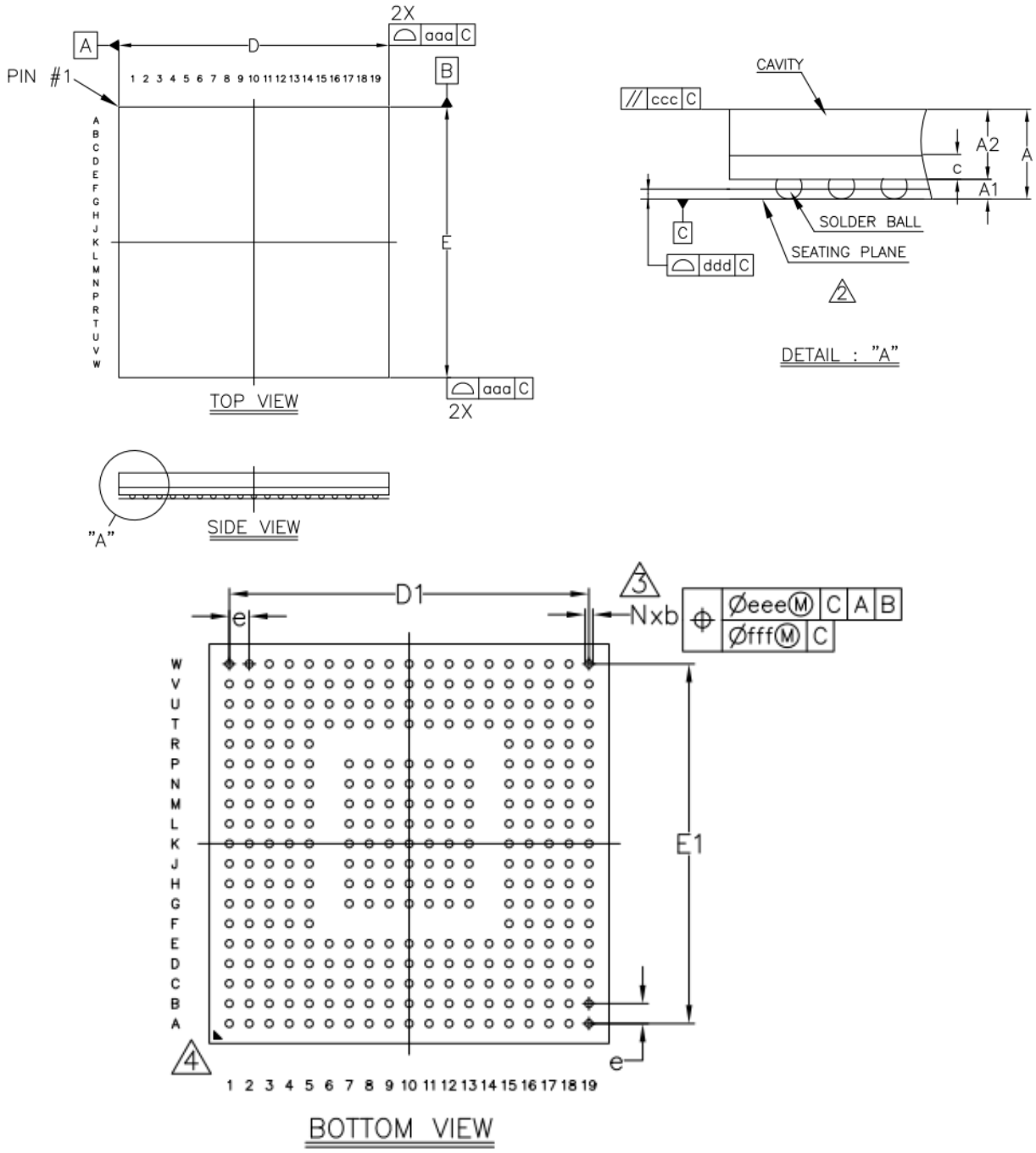
Feature	I350	WX1860
Hardware implemented SM2/SM3/SM4 engine	N	Y
True Random number generator	N	Y

1.7 Power Management Features

Feature	I350	WX1860
Magic packet wake-up enable with unique MAC address	Y	Y
ACPI register set and power down functionality supporting D0 and D3 states	Y	Y
Full wake-up support (APM and ACPI 2.0)	Y	Y
Smart power down at S0 no link and Sx no link	Y	Y
LAN disable functionality	Y	Y
EEE	Y	Y
DMA coalescing	Y	N

2 Pin Interface

2.1 Package Size



Symbol	Min	Nominal	Max
A	1.17	1.24	1.31
A1	0.13	0.18	0.23
A2	1.01	1.06	1.11
c	0.32	0.36	0.40
b	0.20	0.25	0.30
D	12.90	13.00	13.10
E	12.90	13.00	13.10
D1	--	11.70	--
E1	--	11.70	--
e	--	0.65	--
aaa	0.10 BSC		
ccc	0.15 BSC		
ddd	0.13 BSC		
eee	0.15 BSC		
fff	0.08 BSC		
N	327		

Note:

1. Controlling dimension: millimeter
2. Primary datum C and seating plance are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum c.
4. The pattern of pin 1 fiducial is for reference only.
5. Refernce document: JEDEC publication 95 design guide 4.5

2.2 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	GND_PEHY_GD	PE_TX_N_3	GND_PEHY_GD	PE_RX_N_3	PE_RX_N_2	GND_PEHY_GD	PE_TX_N_2	PE_TX_N_1	GND_PEHY_GD	PE_RX_N_1	PE_RX_N_0	GND_PEHY_GD	PE_TX_N_0	UART_SRX	SPI_CLK_DIV_0	N0_GPIO_1	N2_GPIO_1	N3_GPIO_1	GND
B	GND_PEHY_GD	PE_TX_P_3	GND_PEHY_GD	PE_RX_P_3	PE_RX_P_2	GND_PEHY_GD	PE_TX_P_2	PE_TX_P_1	GND_PEHY_GD	PE_RX_P_1	PE_RX_P_0	GND_PEHY_GD	PE_TX_P_0	SPI_CLK_DIV_2	N1_GPIO_1	PE_RST_SEQ	SPI_CLK	JRST_N	JTDI
C	MNG_BSY	MII_MD	VCC33_N3_EFUSE	VCC33_N1_EFUSE	VCC33_N0_EFUSE	GND_TS_GND33A	VCC33A_TDC	PE_REF_CLK_P	GND_PEHY_GD	PE_PHY_RESREF	GND_PEHY_GD	PRB_HIT	PRB_CLKOUT	MNG_GPIO_1	SPI_SI	JTMS	N0_DIS_N	N2_DIS_N	JTAG_SEL_1
D	PRB_EN	PCIE_BSY	MII_MDC	VCC33_EFUSE	VCC33_N2_EFUSE	GND_PEHY_GD	VCC11A_PE_VP	PE_REF_CLK_N	VCC11A_PE_VP	GND_PEHY_GD	UART_STX	N0_GPIO_0	N2_GPIO_0	MNG_GPIO_0	PE_AUX_PWR_DET	SPI_CS_N	SPI_SO	JTDO	N2_RGMII_TX_0
E	CLK_TST_SEL_1	CLK_TST_SEL_3	USE_EXT_PHY	CLK_TST_SEL_0	CLK_TST_SEL_2	VCC11A_PE_VPTX3	VCC11A_PE_VPTX2	VCC33A_PE_VPH	VCC11A_PE_VPTX1	VCC11A_PE_VPTX0	VCCK_VMAIN	SPI_CLK_DIV_1	N1_GPIO_0	N3_GPIO_0	PE_WAKE_N	JTAG_SEL_0	N1_DIS_N	N2_RGMII_TX_1	N2_RGMII_RX_1
F	TEST_MODE_0	TEST_MODE_2	MNG_DET	TEST_MODE_1	TEST_SEL										JTCK	N3_DIS_N	N3_RGMII_TX_1	N2_RGMII_TX_2	N2_RGMII_RX_2
G	SEC_DISABLE	SCAN_ENABLE	PERST_N	FLASH_SECTOR	POR_BYPASS		VCC3IO	GND	GND	VCCK	VCC3IO	VCC3IO	GND		N3_RGMII_TX_2	N3_RGMII_TX_0	N3_RGMII_TX_3	N2_RGMII_TX_3	N2_RGMII_RX_3
H	FLASH_BYPASS	SEC_MODE	N1_LED_0	N0_LED_1	N1_LED_2		VCCK	GND	GND	GND	GND	GND	VCCK		N3_RGMII_RX_2	N3_RGMII_RX_0	N3_RGMII_RX_CTL	N2_RGMII_RX_0	N2_RGMII_TXC
J	PXPOR_RES	N0_LED_2	N2_LED_1	N3_LED_0	N3_LED_2		VCC3IO	GND	GND	GND	GND	GND	VCC18IO_25V		N3_RGMII_RX_1	N3_RGMII_TXC	N3_RGMII_MDC	N2_RGMII_TX_CTL	N2_RGMII_RXC
K	N0_LED_0	N1_LED_1	MNG_IC_SMBSUS_N	MNG_IC_CLK	RMII_CSR_DV		VCCK	GND	GND	GND	GND	GND	VCCK		N3_RGMII_RX_3	N3_RGMII_TX_CTL	N3_RGMII_MDIO	N2_RGMII_RX_CTL	N2_RGMII_MDC
L	N2_LED_2	N3_LED_1	RMII_TXD_1	RMII_TX_EN	N0_TS1588_SDP_1		VCC3IO	GND	GND	GND	GND	GND	VCC18IO_25V		N3_RGMII_RXC	N0_RGMII_TX_1	N0_RGMII_TX_0	N1_RGMII_RXC	N2_RGMII_MDIO
M	N2_LED_0	RMII_RXD_0	N0_TS1588_SDP_3	N1_TS1588_SDP_1	N2_TS1588_SDP_3		VCCK	GND	GND	GND	GND	GND	VCCK		N0_RGMII_RX_1	N0_RGMII_TX_3	N0_RGMII_TX_2	N1_RGMII_MDIO	N1_RGMII_TX_0
N	MNG_IC_SMBALT_N	VCC11A_PLL	GND11A_PLL	N2_TS1588_SDP_1	N3_TS1588_SDP_3		GND	VCC33A_GIGA	GND	VCC33A_GIGA	GND	VCC33A_GIGA	VCC33A_GIGA		N0_RGMII_RXC	N0_RGMII_TXC	N0_RGMII_RX_0	N1_RGMII_RX_3	N1_RGMII_TX_2
P	MNG_IC_DATA	OSC_IO	N1_TS1588_SDP_3	GND	GND		VCC11A_A10	GND	VCC11A_A10	GND	VCC11A_A10	GND	VCC11A_A10		N0_RGMII_MDC	N0_RGMII_RX_2	N0_RGMII_RX_3	N1_RGMII_RX_0	N1_RGMII_TX_1
R	RMII_REF_CLK	OSC_I	N3_TS1588_SDP_0	N3_TS1588_SDP_1	GND										GND	N0_RGMII_TX_CTL	N0_RGMII_RX_CTL	N1_RGMII_RX_2	N1_RGMII_MDC
T	RMII_TXD_0	N0_TS1588_SDP_0	N3_TS1588_SDP_2	GND	VCC11A_CEN	GND	VCCK	GND	VCCK	GND	VCCK	GND	VCCK	GND	VCC33A_CEN	GND	N0_RGMII_MDIO	N1_RGMII_TX_CTL	N1_RGMII_RX_CTL
U	RMII_RXD_1	N1_TS1588_SDP_2	N2_TS1588_SDP_0	GND	G0_RTT	N0_GPHY_RSET	G0_OPIN_PAD	G1_RTT	N1_GPHY_RSET	G1_OPIN_PAD	G2_RTT	N2_GPHY_RSET	G2_OPIN_PAD	G3_RTT	N3_GPHY_RSET	G3_OPIN_PAD	GND	N1_RGMII_TXC	N1_RGMII_TX_3
V	N0_TS1588_SDP_2	N1_TS1588_SDP_0	N0_MDI_P_3	N0_MDI_P_2	N0_MDI_P_1	N0_MDI_P_0	N1_MDI_P_3	N1_MDI_P_2	N1_MDI_P_1	N1_MDI_P_0	N2_MDI_P_3	N2_MDI_P_2	N2_MDI_P_1	N2_MDI_P_0	N3_MDI_P_3	N3_MDI_P_2	N3_MDI_P_1	N3_MDI_P_0	N1_RGMII_RX_1
W	GND	N2_TS1588_SDP_2	N0_MDI_N_3	N0_MDI_N_2	N0_MDI_N_1	N0_MDI_N_0	N1_MDI_N_3	N1_MDI_N_2	N1_MDI_N_1	N1_MDI_N_0	N2_MDI_N_3	N2_MDI_N_2	N2_MDI_N_1	N2_MDI_N_0	N3_MDI_N_3	N3_MDI_N_2	N3_MDI_N_1	N3_MDI_N_0	GND

Figure 1 Ball Map

2.3 Pin Descrption

2.3.1 Misc Interface

芯片采用 3.3V LVCMOS IO 电平标准。输出最大驱动电流 16mA。列表中 Pull 状态表示内部上下拉电阻状态，上下拉电阻值为 75KΩ。Misc 信号有内部上下拉，正常模式下可以悬空。需保留调试模式时，可以加外部电阻。MDI/RGMII/GPIO 信号，端口不用时都可以悬空。

Name	Location	Direction	Pull	Description
prb_en	D1	IN	Down	用于调试，N/C
prb_hit	C12	OUT		用于调试，N/C
prb_clkout	C13	OUT		用于调试，建议加测试点
pcie_bsy	D2	OUT		高有效信号，用于指示 PCIe 连接上有数据传输。

Name	Location	Direction	Pull	Description
mng_bsy	C1	OUT		高有效信号用于指示 NCSI 接口上的数据传输。
scan_enable	G2	IN	Down	用于 DFT 测试。正常模式 N/C。
test_sel	F5	IN	Down	用于调试，N/C
test_mode_0	F1	IN	Down	
test_mode_1	F4	IN	Down	
test_mode_2	F2	IN	Down	
jtag_sel_0	E16	IN	Down	选择 JTAG 接口的使用模块，2'b11 把芯片 JTAG 接口连接在内部 CPU，其它值用于调试。
jtag_sel_1	C19	IN	Down	
clk_tst_sel_0	E4	IN	Down	用于调试，N/C
clk_tst_sel_1	E1	IN	Down	
clk_tst_sel_2	E5	IN	Down	
clk_tst_sel_3	E2	IN	Down	
flash_sector	G4	IN	Down	选择用于初始化的 flash sector， N/C 0-64KB sector 1-256KB sector
flash_bypass	H1	IN	Down	跳过 flash 初始化，用于调试，N/C
mng_det	F3	IN	Up	用于调试， N/C
sec_disable	G1	IN	Down	用于调试，N/C
use_ext_phy	E3	IN	Down	高有效信号。有效时 4 个网口都选择用外部 RGMII PHY，否则 4 个网口都用内部 PHY。
xtal_in	R2	IN		外部无源晶振的输入，也可以直接输入 25MHz 的有源时钟信号。
xtal_out	P2	OUT		输出信号用于连接外部无源晶振。
sec_mode	H2	IN	Up	用于调试， N/C
pe_rst_seq	B16	IN	Down	用于调试，N/C
pe_aux_pwr_det	D15	IN	Down	使用 WoL 功能时拉高，其他模式为低。 支持 WoL 时，支持 D0，D3hot，D3cold。D3 状态下，网口不可通信，NC/SI 可用。不支持 WoL 时，支持到 D0，D3hot，D3cold。PCIe clock 与 WOL 无关，只在 D3cold 时由系统判断。具体内容参考 PCIe Base spec。

2.3.2 Internal PHY #0

Name	Location	Direction	Pull	Description
n0_gphy_rset	U6	A		网口#0 参考电阻接口，通过 2.49KΩ±1%接地
n0_led_0	K1	OUT		LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.
n0_led_1	H4	OUT		LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.
n0_led_2	J2	OUT		LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.
n0_mdi_p_0	V6	A		In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
n0_mdi_n_0	W6	A		
n0_mdi_p_1	V5	A		In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.
n0_mdi_n_1	W5	A		
n0_mdi_p_2	V4	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n0_mdi_n_2	W4	A		
n0_mdi_p_3	V3	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n0_mdi_n_3	W3	A		

2.3.3 RGMII PHY #0

Name	Location	Direction	Pull	Description
n0_rgmii_tx_0	L17	OUT		网口#0 RGMII 发送数据接口
n0_rgmii_tx_1	L16	OUT		
n0_rgmii_tx_2	M17	OUT		

Name	Location	Direction	Pull	Description
n0_rgmii_tx_3	M16	OUT		
n0_rgmii_rx_0	N17	IN/OUT		网口#0 RGMII 接收数据接口
n0_rgmii_rx_1	M15	IN/OUT		
n0_rgmii_rx_2	P16	IN/OUT		
n0_rgmii_rx_3	P17	IN/OUT		
n0_rgmii_txc	N16	OUT		网口#0 RGMII 发送控制接口
n0_rgmii_tx_ctl	R16	OUT		
n0_rgmii_rxc	N15	IN	Down	网口#0 RGMII 接收控制接口
n0_rgmii_rx_ctl	R17	IN	Down	
n0_rgmii_mdc	P15	OUT		网口#0 RGMII MDIO 接口，MDIO 信号需外部上拉 1.5-10Kohm 电阻。
n0_rgmii_mdio	T17	IN/OUT		

2.3.4 Internal PHY #1

Name	Location	Direction	Pull	Description
n0_dis_n	C17	IN	Up	网口#0 不使能信号，低有效
n1_dis_n	E17	IN	Up	网口#1 不使能信号，低有效
n2_dis_n	C18	IN	Up	网口#2 不使能信号，低有效
n3_dis_n	F16	IN	Up	网口#3 不使能信号，低有效
n1_gphy_rset	U9	A		网口#1 参考电阻接口，通过 2.49KΩ±1%接地
n1_led_0	H3	OUT		LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.
n1_led_1	K2	OUT		LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.
n1_led_2	H5	OUT		LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.
n1_mdi_p_0	V10	A		In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
n1_mdi_n_0	W10	A		

Name	Location	Direction	Pull	Description
n1_mdi_p_1	V9	A		In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.
n1_mdi_n_1	W9	A		
n1_mdi_p_2	V8	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n1_mdi_n_2	W8	A		
n1_mdi_p_3	V7	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n1_mdi_n_3	W7	A		

2.3.5 RGMII PHY #1

Name	Location	Direction	Pull	Description
n1_rgmii_tx_0	M19	OUT		网口#1 RGMII 发送数据接口
n1_rgmii_tx_1	P19	OUT		
n1_rgmii_tx_2	N19	OUT		
n1_rgmii_tx_3	U19	OUT		
n1_rgmii_rx_0	P18	IN/OUT		网口#1 RGMII 接收数据接口
n1_rgmii_rx_1	V19	IN/OUT		
n1_rgmii_rx_2	R18	IN/OUT		
n1_rgmii_rx_3	N18	IN/OUT		
n1_rgmii_txc	U18	OUT		网口#1 RGMII 发送控制接口
n1_rgmii_tx_ctl	T18	OUT		
n1_rgmii_rxc	L18	IN	Down	网口#1 RGMII 接收控制接口
n1_rgmii_rx_ctl	T19	IN	Down	
n1_rgmii_mdc	R19	OUT		网口#1 RGMII MDIO 接口，MDIO 信号需外部上拉 1.5-10Kohm 电阻。
n1_rgmii_mdio	M18	IN/OUT		

2.3.6 Internal PHY #2 (4-Port only)

Name	Location	Direction	Pull	Description
n2_gphy_rset	U12	A		网口#2 参考电阻接口，通过 2.49KΩ±1%接地
n2_led_0	M1	OUT		LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.
n2_led_1	J3	OUT		LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.
n2_led_2	L1	OUT		LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.
n2_mdi_p_0	V14	A		In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
n2_mdi_n_0	W14	A		
n2_mdi_p_1	V13	A		In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.
n2_mdi_n_1	W13	A		
n2_mdi_p_2	V12	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n2_mdi_n_2	W12	A		
n2_mdi_p_3	V11	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n2_mdi_n_3	W11	A		

2.3.7 RGMII PHY #2 (4-Port only)

Name	Location	Direction	Pull	Description
n2_rgmii_tx_0	D19	OUT		网口#2 RGMII 发送数据接口
n2_rgmii_tx_1	E18	OUT		
n2_rgmii_tx_2	F18	OUT		

Name	Location	Direction	Pull	Description
n2_rgmii_tx_3	G18	OUT		
n2_rgmii_rx_0	H18	IN		网口#2 RGMII 接收数据接口
n2_rgmii_rx_1	E19	IN		
n2_rgmii_rx_2	F19	IN		
n2_rgmii_rx_3	G19	IN		
n2_rgmii_txc	H19	OUT		网口#2 RGMII 发送控制接口
n2_rgmii_tx_ctl	J18	OUT		
n2_rgmii_rxc	J19	IN	Down	网口#2 RGMII 接收控制接口
n2_rgmii_rx_ctl	K18	IN	Down	
n2_rgmii_mdc	K19	OUT		网口#2 RGMII MDIO 接口，MDIO 信号需外部上拉 1.5-10Kohm 电阻。
n2_rgmii_mdio	L19	IN/OUT		

2.3.8 Internal PHY #3 (4-Port only)

Name	Location	Direction	Pull	Description
n3_gphy_rset	U15	A		网口#3 参考电阻接口，通过 2.49KΩ±1%接地
n3_led_0	J4	OUT		LED_0, Programmable LED which indicates by default activity, active high. Blink time 20-60ms adjustable, active high/low adjustable.
n3_led_1	L2	OUT		LED_1, Programmable LED which indicates by default a 100Mbps Link, active high.
n3_led_2	J5	OUT		LED_2, Programmable LED which indicates by default a 1000Mbps Link, active high.
n3_mdi_p_0	V18	A		In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
n3_mdi_n_0	W18	A		
n3_mdi_p_1	V17	A		In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transimit pair in 10Base-T and 100Base-TX.
n3_mdi_n_1	W17	A		

Name	Location	Direction	Pull	Description
n3_mdi_p_2	V16	A		In MDI mode, this is the third pair in 1000Base-T, i.e.,the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
n3_mdi_n_2	W16	A		
n3_mdi_p_3	V15	A		In MDI mode, this is the Fourth pair in 1000Base-T, i.e.,the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
n3_mdi_n_3	W15	A		

2.3.9 RGMII PHY #3 (4-Port only)

Name	Location	Direction	Pull	Description
n3_rgmii_tx_0	G16	OUT		网口#3 RGMII 发送数据接口
n3_rgmii_tx_1	F17	OUT		
n3_rgmii_tx_2	G15	OUT		
n3_rgmii_tx_3	G17	OUT		
n3_rgmii_rx_0	H16	IN/OUT		网口#3 RGMII 接收数据接口
n3_rgmii_rx_1	J15	IN/OUT		
n3_rgmii_rx_2	H15	IN/OUT		
n3_rgmii_rx_3	K15	IN/OUT		
n3_rgmii_txc	J16	OUT		网口#3 RGMII 发送控制接口
n3_rgmii_tx_ctl	K16	OUT		
n3_rgmii_rxc	L15	IN	Down	网口#3 RGMII 接收控制接口
n3_rgmii_rx_ctl	H17	IN	Down	
n3_rgmii_mdc	J17	OUT		网口#3 RGMII MDIO 接口，MDIO 信号需外部上拉 1.5-10Kohm 电阻。
n3_rgmii_mdio	K17	IN/OUT		

2.3.10 GPIO

Name	Location	Direction	Pull	Description
n0_gpio_0	D12	IN/OUT		网口#0 GPIO 0，可用于复位输出或中断输入
n0_gpio_1	A16	IN/OUT		网口#0 GPIO 1，可用于复位输出或中断输入
n1_gpio_0	E13	IN/OUT		网口#1 GPIO 0，可用于复位输出或中断输入

Name	Location	Direction	Pull	Description
n1_gpio_1	B15	IN/OUT		网口#1 GPIO 1，可用于复位输出或中断输入
n2_gpio_0	D13	IN/OUT		网口#2 GPIO 0，可用于复位输出或中断输入
n2_gpio_1	A17	IN/OUT		网口#2 GPIO 1，可用于复位输出或中断输入
n3_gpio_0	E14	IN/OUT		网口#3 GPIO 0，可用于复位输出或中断输入
n3_gpio_1	A18	IN/OUT		网口#3 GPIO 1，可用于复位输出或中断输入
mng_gpio_0	D14	IN/OUT		CPU GPIO 0，可用于复位输出或中断输入
mng_gpio_1	C14	IN/OUT		片 CPU GPIO 1，可用于复位输出或中断输入

2.3.11 Management Interface

管理 接口可以作为 MII 接口外接 PHY 使用，也可以作为 NCSI 接 BMC 芯片使用。

在连接外部 mac 时，SMBUS mode 和 NC-SI mode 可以同时支持。

Name	Location	Direction	Pull	Description
uart_srx	A14	IN	Down	片上 CPU UART 接口，用于调试，可访问 CPU 内部寄存器信息。
uart_stx	D11	OUT		
mng_ic_clk	K4	IN/OD	Up	片上 CPU I2C 接口时钟信号，该信号在任何状态下都支持，与 pe_aux_pwr_det 无关。
mng_ic_data	P1	IN/OD	Up	片上 CPU I2C 接口数据信号，该信号在任何状态下都支持，与 pe_aux_pwr_det 无关。
mng_ic_smbsus_n	K3	IN/OUT	Up	片上 CPU I2C 接口挂起信号
mng_ic_smbalt_n	N1	IN/OD	Up	片上 CPU I2C 接口输出中断信号
rmii_ref_clk/ ncsi_ref_clk	R1	IN	Down	NC-SI Reference Clock Input – Synchronous clock reference for receive, transmit and control interface. It is a 50MHz clock +/- 100 ppm.
rmii_csr_dv/ ncsi_ tx_en	K5	IN	Down	Transmit Enable
rmii_rxd_0/ ncsi_txd_0	M2	IN	Down	Transmit data signals from BMC to WX1860
rmii_rxd_1/ ncsi_txd_1	U1	IN	Down	
rmii_tx_en/	L4	OUT		Carrier Sense/Receive Data Valid

Name	Location	Direction	Pull	Description
ncsi_csr_dv				
rmii_txd_0/ ncsi_rxd_0	T1	OUT		Received data signals from WX1860 to BMC
rmii_txd_1/ ncsi_rxd_1	L3	OUT		
mii_mdc	D3	OUT		MII MDIO 接口。
mii_md	C2	IN /OUT		

2.3.12 TS1588 Pins

Name	Location	Direction	Pull	Description
n0_ts1588_sdp_0	T2	IN/OUT		网口#0 TS1588 GPIO，结合芯片定时器，用于产生可配置时钟、脉冲、电平、集外部事件、基于外部事件产生中断。不使用可以悬空。
n0_ts1588_sdp_1	L5	IN/OUT		
n0_ts1588_sdp_2	V1	IN/OUT		
n0_ts1588_sdp_3	M3	IN/OUT		
n1_ts1588_sdp_0	V2	IN/OUT		网口#1 TS1588 GPIO，结合芯片定时器，用于产生可配置时钟、脉冲、电平、集外部事件、基于外部事件产生中断。不使用可以悬空。
n1_ts1588_sdp_1	M4	IN/OUT		
n1_ts1588_sdp_2	U2	IN/OUT		
n1_ts1588_sdp_3	P3	IN/OUT		
n2_ts1588_sdp_0	U3	IN/OUT		网口#2 TS1588 GPIO，结合芯片定时器，用于产生可配置时钟、脉冲、电平、集外部事件、基于外部事件产生中断。不使用可以悬空。
n2_ts1588_sdp_1	N4	IN/OUT		
n2_ts1588_sdp_2	W2	IN/OUT		
n2_ts1588_sdp_3	M5	IN/OUT		
n3_ts1588_sdp_0	R3	IN/OUT		网口#3 TS1588 GPIO，结合芯片定时器，用于产生可配置时钟、脉冲、电平、集外部事件、基于外部事件产生中断。不使用可以悬空。
n3_ts1588_sdp_1	R4	IN/OUT		
n3_ts1588_sdp_2	T3	IN/OUT		
n3_ts1588_sdp_3	N5	IN/OUT		

2.3.13 PCIe Interface

Name	Location	Direction	Pull	Description
pe_wake_n	E15	OD	Up	PCIe WAKE# 信号，低有效，使用 WOL 功能时需使能此信号。
pxpor_res	J1	IN	Down	复位信号输入，POR_BYPASS= 0: 使用片内上电复位，此时 PXPOR_RES 引脚悬空。 POR_BYPASS= 1: 使用外部复位。外部复位从 PXPOR_RES 接入。
por_bypass	G5	IN	Down	片内上电复位控制电路旁路使能，高有效。有效时，片内上电复位控制电路被旁路，片内不再产生上电复位信号，芯片的上电复位信号来自 pxpor_res，此时 pxpor_res 作为低有效信号。
perst_n	G3	IN		PCIe PERST#信号，低有效。
pe_phy_resref	C10	A		PCIe PHY 参考电阻，200Ω (1% ,±100 ppm/°C)
pe_ref_clk_p	C8	A-in		PCIe 100MHz 参考时钟，来自 PCIe slot。
pe_ref_clk_n	D8	A-in		
pe_tx_p_0	B13	A-out		PCIe PHY Gen2x4 差分收发信号
pe_tx_n_0	A13	A-out		
pe_tx_p_1	B8	A-out		
pe_tx_n_1	A8	A-out		
pe_tx_p_2	B7	A-out		
pe_tx_n_2	A7	A-out		
pe_tx_p_3	B2	A-out		
pe_tx_n_3	A2	A-out		
pe_rx_p_0	B11	A-in		
pe_rx_n_0	A11	A-in		
pe_rx_p_1	B10	A-in		
pe_rx_n_1	A10	A-in		
pe_rx_p_2	B5	A-in		
pe_rx_n_2	A5	A-in		
pe_rx_p_3	B4	A-in		
pe_rx_n_3	A4	A-in		

2.3.14 SPI flash Interface

Name	Location	Direction	Pull	Description
spi_clk_div_0	A15	IN	Down	用于调试，不支持 WOL 时默认配置 011。支持 WOL 时采用 000。 SPI clock 可以配置为 62.5MHz 的不同分频。 000: ”divide by 2”, 31.25MHz 001: “divide by 4” 15.625MHz 010: “divide by 6”10.417MHz 011: “divide by 8”7.8125MHz 100: “divide by 10”6.25MHz 101: “divide by 16”3.90625MHz 110-111 not used.
spi_clk_div_1	E12	IN	Down	
spi_clk_div_2	B14	IN	Down	
spi_clk	B17	OUT		SPI flash 接口信号
spi_cs_n	D16	OUT		
spi_si	C15	IN	Down	
spi_so	D17	OUT		

2.3.15 JTAG

Name	Location	Direction	Pull	Description
jrst_n	B18	IN	Down	JTAG 接口信号
jtck	F15	IN	Down	
jtdi	B19	IN	Up	
jtdo	D18	OUT		
jtms	C16	IN/OUT	Up	

2.3.16 Power Supply

管脚名称	管脚	描述
VCC33_N0_EFUSE	C5	EFUSE 模拟 3.3V
VCC33_N1_EFUSE	C4	
VCC33_N2_EFUSE	D5	
VCC33_N3_EFUSE	C3	

VCC33_EFUSE	D4	
VCC33A_TDC	C7	内部温度传感器模拟 3.3V
VCC33A_PE_VPH	E8	PCIe 模拟 3.3V
VCC3IO	G7 G11 G12 J7 L7	RGMII、Misc 数字 IO 3.3V
VCC33A_GIGA	N8 N10 N12 N13	MDI 网口模拟 3.3V
VCC33A_CEN	T15	MDI 网口模拟 3.3V
VCCK_VMAIN	E11	内核数字电源 1.1V
VCCK_AUX	G10 H7 H13 K7 K13 M7 M13 T7 T9 T11 T13	内核数字备用电源 1.1V
VCC11A_PE_VP	D7 D9	PCIe 模拟电源 1.1V
VCC11A_PE_VPTX0	E10	
VCC11A_PE_VPTX1	E9	
VCC11A_PE_VPTX2	E7	
VCC11A_PE_VPTX3	E6	
VCC11A_A10	P7 P9 P11 P13	MDI 网口模拟电源 1.1V
VCC11A_PLL	N2	PLL 电源，模拟 1.1V
VCC11A_CEN	T5	MDI 网口模拟 1.1V
VCC18IO_25V	J13	RGMII 数字 IO，目前 1.8V/2.5V 模式不支持，需接到 3.3V。
VCC18IO_25V	L13	

2.3.17 Ground

管脚名称	管脚	描述
GND	A1 A3 A6 A9 A12 B1 B3 B6 B9 B12 C9 C11 D6 D10 G8 G9 G13 H8 H9 H10 H11 H12 J8 J9 J10 J11 J12 K8 K9 K10 K11 K12 A19 L8 L9 L10 L11 L12 M8 M9 M10 M11 M12 N7 N9 N11 P4 P5 P8 P10 P12 R5 R15 T4 T6 T8 T10 T12 T14 T16 U4 U17 W1 W19	电源地
GND_PLL	N3	PLL 电源，通过磁珠单点接地，目的是为了隔离电源模拟地和数字地。

管脚名称	管脚	描述
GND_TS	C6	内部 Thermal sensor 电源，通过磁珠单点接地，目的是为了隔离电源模拟地和数字地。

2.4 Ball List ordered by Ball location

Pin	Netname	Description
A1	GND_PEPHY_GD	
A2	PE_TX_N_3	PCIe 5Gbps SerDes
A3	GND_PEPHY_GD	
A4	PE_RX_N_3	PCIe 5Gbps SerDes
A5	PE_RX_N_2	PCIe 5Gbps SerDes
A6	GND_PEPHY_GD	
A7	PE_TX_N_2	PCIe 5Gbps SerDes
A8	PE_TX_N_1	PCIe 5Gbps SerDes
A9	GND_PEPHY_GD	
A10	PE_RX_N_1	PCIe 5Gbps SerDes
A11	PE_RX_N_0	PCIe 5Gbps SerDes
A12	GND_PEPHY_GD	
A13	PE_TX_N_0	PCIe 5Gbps SerDes
A14	UART_SRX	UART
A15	SPI_CLK_DIV_0	SPI clock divider bit[0]
A16	N0_GPIO_1	Lan0 GPIO bit[1]
A17	N2_GPIO_1	Lan2 GPIO bit[1]
A18	N3_GPIO_1	Lan3 GPIO bit[1]
A19	GND	
B1	GND_PEPHY_GD	
B2	PE_TX_P_3	PCIe 5Gbps SerDes
B3	GND_PEPHY_GD	
B4	PE_RX_P_3	PCIe 5Gbps SerDes
B5	PE_RX_P_2	PCIe 5Gbps SerDes
B6	GND_PEPHY_GD	
B7	PE_TX_P_2	PCIe 5Gbps SerDes
B8	PE_TX_P_1	PCIe 5Gbps SerDes
B9	GND_PEPHY_GD	
B10	PE_RX_P_1	PCIe 5Gbps SerDes

Pin	Netname	Description
B11	PE_RX_P_0	PCIe 5Gbps SerDes
B12	GND_PEPHY_GD	
B13	PE_TX_P_0	PCIe 5Gbps SerDes
B14	SPI_CLK_DIV_2	SPI clock divider bit[2]
B15	N1_GPIO_1	Lan1 GPIO bit[1]
B16	PE_RST_SEQ	PCIe reset sequence control.
B17	SPI_CLK	SPI flash clock, max clock frequency is 50MHz
B18	JRST_N	JTAG reset
B19	JTDI	JTAG TDI
C1	MNG_BSY	Management busy indication
C2	MII_MD	NCSI PHY MDIO
C3	VCC33_N3_EFUSE	
C4	VCC33_N1_EFUSE	
C5	VCC33_N0_EFUSE	
C6	GND_TS_GND33A	
C7	VCC33A_TDC	
C8	PE_REF_CLK_P	PCIe 100MHz reference clock
C9	GND_PEPHY_GD	
C10	PE_PHY_RESREF	PCIe reference resistor
C11	GND_PEPHY_GD	
C12	PRB_HIT	Probe hit 用于调试
C13	PRB_CLKOUT	Probe clock out 用于调试
C14	MNG_GPIO_1	Managment GPIO bit [1]
C15	SPI_SI	SPI flash SI
C16	JTMS	JTAG JMS
C17	N0_DIS_N	Active low Lan0 disable
C18	N2_DIS_N	Active low Lan2 disable
C19	JTAG_SEL_1	JTAG select bit[1]
D1	PRB_EN	Probe enable, 0 for normal function
D2	PCIE_BSY	PCIe link busy indication
D3	MII_MDC	NCSI PHY MDIO
D4	VCC33_EFUSE	
D5	VCC33_N2_EFUSE	
D6	GND_PEPHY_GD	
D7	VCC11A_PE_VP	
D8	PE_REF_CLK_N	PCIe PHY reference clock
D9	VCC11A_PE_VP	

Pin	Netname	Description
D10	GND_PEPHY_GD	
D11	UART_STX	UART
D12	N0_GPIO_0	
D13	N2_GPIO_0	
D14	MNG_GPIO_0	
D15	PE_AUX_PWR_DET	PCIe Aux power available
D16	SPI_CS_N	SPI flash CS_N
D17	SPI_SO	SPI flash SO
D18	JTDO	JTAG JTDO
D19	N2_RGMII_TX_0	RGMII interface
E1	CLK_TST_SEL_1	Test clock selection, 用于调试 only
E2	CLK_TST_SEL_3	Test clock selection, 用于调试 only
E3	USE_EXT_PHY	External PHY selection, 1'b0 to use internal 1000Base-T PHY, 1'b1 to use external RGMII PHY. It controls all 4 ports.
E4	CLK_TST_SEL_0	Test clock selection, 用于调试 only
E5	CLK_TST_SEL_2	Test clock selection, 用于调试 only
E6	VCC11A_PE_VPTX3	
E7	VCC11A_PE_VPTX2	
E8	VCC33A_PE_VPH	
E9	VCC11A_PE_VPTX1	
E10	VCC11A_PE_VPTX0	
E11	VCCK_VMAIN	
E12	SPI_CLK_DIV_1	SPI clock divider control bit[1]
E13	N1_GPIO_0	Lan1 GPIO bit[0]
E14	N3_GPIO_0	Lan3 GPIO bit[0]
E15	PE_WAKE_N	Active low WAKE# on PCIe slot.
E16	JTAG_SEL_0	JTAG selection bit[0]
E17	N1_DIS_N	Active low Lan1 disable
E18	N2_RGMII_TX_1	RGMII interface
E19	N2_RGMII_RX_1	RGMII interface
F1	TEST_MODE_0	Test mode, 0 for normal function
F2	TEST_MODE_2	Test mode, 0 for normal function
F3	MNG_DET	Management available, 1 for normal function
F4	TEST_MODE_1	Test mode, 0 for normal function
F5	TEST_SEL	Test selection, 0 for normal function
F15	JTCK	JTAG TCK
F16	N3_DIS_N	Active low Lan3 disable

Pin	Netname	Description
F17	N3_RGMII_TX_1	RGMII interface
F18	N2_RGMII_TX_2	RGMII interface
F19	N2_RGMII_RX_2	RGMII interface
G1	SEC_DISABLE	1'b1 to disable IPsec and LinkSec
G2	SCAN_ENABLE	For DFT, 0 for normal function
G3	PERST_N	PERST# at PCIe slot
G4	FLASH_SECTOR	0 for 64KB, 1 for 256KB
G5	POR_BYPASS	1 to by pass chip internal POR module and use PXPOR_RES as active low power on reset
G7	VCC3IO	
G8	GND	
G9	GND	
G10	VCCK	
G11	VCC3IO	
G12	VCC3IO	
G13	GND	
G15	N3_RGMII_TX_2	RGMII interface
G16	N3_RGMII_TX_0	RGMII interface
G17	N3_RGMII_TX_3	RGMII interface
G18	N2_RGMII_TX_3	RGMII interface
G19	N2_RGMII_RX_3	RGMII interface
H1	FLASH_BYPASS	0 for normal function
H2	SEC_MODE	1 to enable sec mode
H3	N1_LED_0	Lan LED
H4	N0_LED_1	Lan LED
H5	N1_LED_2	Lan LED
H7	VCCK	
H8	GND	
H9	GND	
H10	GND	
H11	GND	
H12	GND	
H13	VCCK	
H15	N3_RGMII_RX_2	RGMII interface
H16	N3_RGMII_RX_0	RGMII interface
H17	N3_RGMII_RX_CTL	RGMII interface
H18	N2_RGMII_RX_0	RGMII interface
H19	N2_RGMII_TXC	RGMII interface

Pin	Netname	Description
J1	PXPOR_RES	Active High reset to reset chip intern POR. When POR_BYPASS=1, it is the active low power on reset.
J2	N0_LED_2	Lan LED
J3	N2_LED_1	Lan LED
J4	N3_LED_0	Lan LED
J5	N3_LED_2	Lan LED
J7	VCC3IO	
J8	GND	
J9	GND	
J10	GND	
J11	GND	
J12	GND	
J13	VCC18IO_25V	
J15	N3_RGMII_RX_1	RGMII interface
J16	N3_RGMII_TXC	RGMII interface
J17	N3_RGMII_MDC	RGMII MDIO for extern PHY control
J18	N2_RGMII_TX_CTL	RGMII interface
J19	N2_RGMII_RXC	RGMII interface
K1	N0_LED_0	Lan LED
K2	N1_LED_1	Lan LED
K3	MNG_IC_SMBSUS_N	SMbus for management
K4	MNG_IC_CLK	SMbus for management
K5	RMII_CSR_DV	NCSI interface
K7	VCCK	
K8	GND	
K9	GND	
K10	GND	
K11	GND	
K12	GND	
K13	VCCK	
K15	N3_RGMII_RX_3	RGMII interface
K16	N3_RGMII_TX_CTL	RGMII interface
K17	N3_RGMII_MDIO	RGMII MDIO for extern PHY control
K18	N2_RGMII_RX_CTL	RGMII interface
K19	N2_RGMII_MDC	RGMII MDIO for extern PHY control
L1	N2_LED_2	Lan LED
L2	N3_LED_1	Lan LED
L3	RMII_TXD_1	NCSI interface

Pin	Netname	Description
L4	RMII_TX_EN	NCSI interface
L5	N0_TS1588_SDP_1	TS1588 GPIO
L7	VCC3IO	
L8	GND	
L9	GND	
L10	GND	
L11	GND	
L12	GND	
L13	VCC18IO_25V	
L15	N3_RGMII_RXC	RGMII interface
L16	N0_RGMII_TX_1	RGMII interface
L17	N0_RGMII_TX_0	RGMII interface
L18	N1_RGMII_RXC	RGMII interface
L19	N2_RGMII_MDIO	RGMII MDIO for extern PHY control
M1	N2_LED_0	Lan LED
M2	RMII_RXD_0	NCSI interface
M3	N0_TS1588_SDP_3	TS1588 GPIO
M4	N1_TS1588_SDP_1	TS1588 GPIO
M5	N2_TS1588_SDP_3	TS1588 GPIO
M7	VCCK	
M8	GND	
M9	GND	
M10	GND	
M11	GND	
M12	GND	
M13	VCCK	
M15	N0_RGMII_RX_1	RGMII interface
M16	N0_RGMII_TX_3	RGMII interface
M17	N0_RGMII_TX_2	RGMII interface
M18	N1_RGMII_MDIO	RGMII MDIO for extern PHY control
M19	N1_RGMII_TX_0	RGMII interface
N1	MNG_IC_SMBALT_N	SMbus for management
N2	VCC11A_PLL	
N3	GND11A_PLL	
N4	N2_TS1588_SDP_1	TS1588 GPIO
N5	N3_TS1588_SDP_3	TS1588 GPIO
N7	GND	
N8	VCC33A_GIGA	

Pin	Netname	Description
N9	GND	
N10	VCC33A_GIGA	
N11	GND	
N12	VCC33A_GIGA	
N13	VCC33A_GIGA	
N15	N0_RGMII_RXC	RGMII interface
N16	N0_RGMII_TXC	RGMII interface
N17	N0_RGMII_RX_0	RGMII interface
N18	N1_RGMII_RX_3	RGMII interface
N19	N1_RGMII_TX_2	RGMII interface
P1	MNG_IC_DATA	SMbus for management
P2	OSC_IO	External oscillator
P3	N1_TS1588_SDP_3	TS1588 GPIO
P4	GND	
P5	GND	
P7	VCC11A_A10	
P8	GND	
P9	VCC11A_A10	
P10	GND	
P11	VCC11A_A10	
P12	GND	
P13	VCC11A_A10	
P15	N0_RGMII_MDC	RGMII MDIO for extern PHY control
P16	N0_RGMII_RX_2	RGMII interface
P17	N0_RGMII_RX_3	RGMII interface
P18	N1_RGMII_RX_0	RGMII interface
P19	N1_RGMII_TX_1	RGMII interface
R1	RMII_REF_CLK	NCSI interface
R2	OSC_I	External oscillator
R3	N3_TS1588_SDP_0	TS1588 GPIO
R4	N3_TS1588_SDP_1	TS1588 GPIO
R5	GND	
R15	GND	
R16	N0_RGMII_TX_CTL	RGMII interface
R17	N0_RGMII_RX_CTL	RGMII interface
R18	N1_RGMII_RX_2	RGMII interface
R19	N1_RGMII_MDC	RGMII MDIO for extern PHY control
T1	RMII_TXD_0	NCSI interface

Pin	Netname	Description
T2	N0_TS1588_SDP_0	TS1588 GPIO
T3	N3_TS1588_SDP_2	TS1588 GPIO
T4	GND	
T5	VCC11A_CEN	
T6	GND	
T7	VCCK	
T8	GND	
T9	VCCK	
T10	GND	
T11	VCCK	
T12	GND	
T13	VCCK	
T14	GND	
T15	VCC33A_CEN	
T16	GND	
T17	N0_RGMII_MDIO	RGMII MDIO for extern PHY control
T18	N1_RGMII_TX_CTL	RGMII interface
T19	N1_RGMII_RX_CTL	RGMII interface
U1	RMII_RXD_1	NCSI interface
U2	N1_TS1588_SDP_2	TS1588 GPIO
U3	N2_TS1588_SDP_0	TS1588 GPIO
U4	GND	
U5	G0_RTT	
U6	N0_GPHY_RSET	
U7	G0_OPIN_PAD	
U8	G1_RTT	
U9	N1_GPHY_RSET	
U10	G1_OPIN_PAD	
U11	G2_RTT	
U12	N2_GPHY_RSET	
U13	G2_OPIN_PAD	
U14	G3_RTT	
U15	N3_GPHY_RSET	
U16	G3_OPIN_PAD	
U17	GND	
U18	N1_RGMII_TXC	RGMII interface
U19	N1_RGMII_TX_3	RGMII interface
V1	N0_TS1588_SDP_2	TS1588 GPIO

Pin	Netname	Description
V2	N1_TS1588_SDP_0	TS1588 GPIO
V3	N0_MDI_P_3	1000Base-T serdes
V4	N0_MDI_P_2	1000Base-T serdes
V5	N0_MDI_P_1	1000Base-T serdes
V6	N0_MDI_P_0	1000Base-T serdes
V7	N1_MDI_P_3	1000Base-T serdes
V8	N1_MDI_P_2	1000Base-T serdes
V9	N1_MDI_P_1	1000Base-T serdes
V10	N1_MDI_P_0	1000Base-T serdes
V11	N2_MDI_P_3	1000Base-T serdes
V12	N2_MDI_P_2	1000Base-T serdes
V13	N2_MDI_P_1	1000Base-T serdes
V14	N2_MDI_P_0	1000Base-T serdes
V15	N3_MDI_P_3	1000Base-T serdes
V16	N3_MDI_P_2	1000Base-T serdes
V17	N3_MDI_P_1	1000Base-T serdes
V18	N3_MDI_P_0	1000Base-T serdes
V19	N1_RGMII_RX_1	RGMII interface
W1	GND	
W2	N2_TS1588_SDP_2	TS1588 GPIO
W3	N0_MDI_N_3	1000Base-T serdes
W4	N0_MDI_N_2	1000Base-T serdes
W5	N0_MDI_N_1	1000Base-T serdes
W6	N0_MDI_N_0	1000Base-T serdes
W7	N1_MDI_N_3	1000Base-T serdes
W8	N1_MDI_N_2	1000Base-T serdes
W9	N1_MDI_N_1	1000Base-T serdes
W10	N1_MDI_N_0	1000Base-T serdes
W11	N2_MDI_N_3	1000Base-T serdes
W12	N2_MDI_N_2	1000Base-T serdes
W13	N2_MDI_N_1	1000Base-T serdes
W14	N2_MDI_N_0	1000Base-T serdes
W15	N3_MDI_N_3	1000Base-T serdes

Pin	Netname	Description
W16	N3_MDI_N_2	1000Base-T serdes
W17	N3_MDI_N_1	1000Base-T serdes
W18	N3_MDI_N_0	1000Base-T serdes
W19	GND	

3 电气规格

3.1 极限工作条件

参数	Min	Typ	Max	Units
存储温度范围	-65		140	° C
Tj(PN 结温度)	-55		125	° C
VCCK 和 VCC11A	-0.1	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	-0.1	1.1	1.155	V
VCC3IO,VCC33A，VCC33	-0.4	3.3	3.7	V
VCC18IO_25V	-0.4	3.3	3.7	V

Table1 WX1860 极限工作条件

3.2 建议工作条件

参数	Min	Typ	Max	Units
工作温度范围	-40		85	° C
VCCK 和 VCC11A	1.045	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	1.045	1.1	1.155	V
VCC3IO,VCC33A，VCC33	3.135	3.3	3.465	V
VCC18IO_25V	3.135	3.3	3.465	V

Table2 WX1860 建议工作条件

3.3 直流特性

参数	Symbol	Conditions	Min	Typ	Max	Units
IO reference voltage	Vref		3.0	3.3	3.6	V
Input low voltage	Vil				0.8	V
Input high voltage	Vih		2.0			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref-Vref,max	0		200	μA
Output low voltage	Vol	Iol=4mA,Vref=min	0		400	mV
Output high voltage	Voh	IOh=-4mA,Vref=min	2.4		Vref	V

Table2 WX1860 直流特性

3.4 交流特性

3.4.1 NCSI AC Specification

The WX1860 is designed to support the standard DMTF NCSI interface. For NCSI I/F timing specification see the following table.

Symbol	Parameter	Min	Typ	Max	Units
Tckf	NCSI_REF_CLK Frequency		50		MHz
Rdc	NCSI_REF_CLK duty cycle	35		65	%
Racc	NCSI_REF_CLK accuracy			100	ppm
Tco	Clock-to-out (10 pF =< cload <=50 pF) NCSI_RXD[1:0], NCSI_CSR_DV Data valid from NCSI_REF_CLK rising edge	2.5		12.5	ns
Tsu	NCSI_TXD[1:0], NCSI_TX_EN Data Setup to NCSI_CLK_IN rising edge	3			ns
Thold	NCSI_TXD[1:0], NCSI_TX_EN Data hold from NCSI_REF_CLK rising edge	1			ns
Tor	NCSI_RXD[1:0], NCSI_CSR_DV Output Time rise	0.5		6	ns
Tof	NCSI_RXD[1:0], NCSI_CSR_DV Output Time fall	0.5		6	ns
Tckr/Tckf	NCSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

3.5 时钟输入

The 25 MHz reference clock of the WX1860 can be supplied either from a crystal or from an external oscillator. The recommended solution is to use a crystal.

3.5.1 Specification for External Crystal

参数	Condition	Min	Typ	Max	Units
Frequency	-	-	25	-	MHz
Vibration mode			Fundamental		
Frequency Stability	Ta=0-70℃	-30		+30	ppm

Frequency Tolerance	Ta=25℃	-50		+50	ppm
Load Capacitance			20		pf

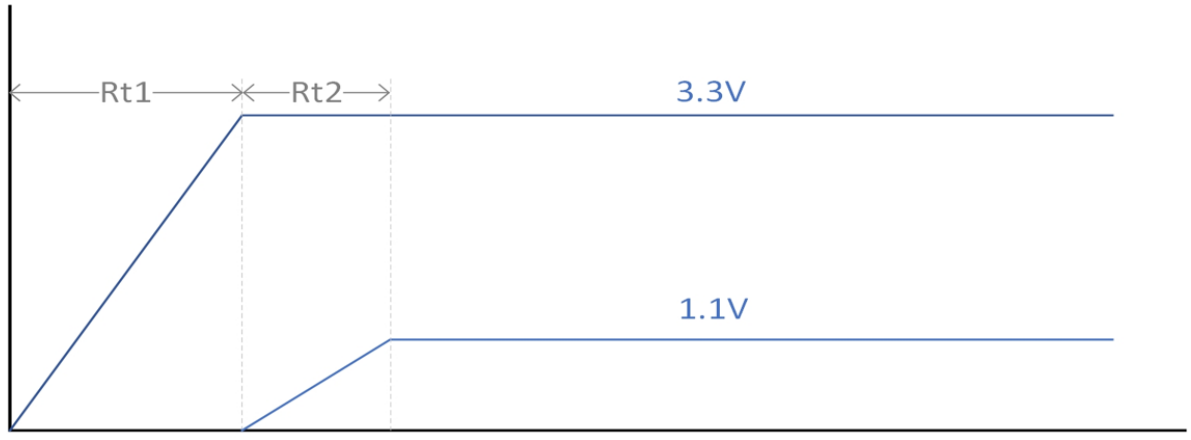
3.5.2 External Clock Oscillator Specification

参数	Condition	Min	Typ	Max	Units
Frequency	-	-	25	-	MHz
Frequency Stability	Ta=0-70℃	-30		+30	ppm
Frequency Tolerance	Ta=25℃	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak-to-peak Jitter				200	ps
Vpeak-to-peak		3.135	3.3	3.465	V
Rise time（10%-90%）				10	ns
Fall time （10%-90%）				10	ns
Operation temperature Range		0		70	℃

Table2 WX1860 外部时钟输入

3.5 上电顺序

根据内部 GPHY IP 的要求，1.1V 不能先于 3.3V 5ms 上电。3.3V rise time 要求大于 1ms。结合我司芯片验证的结果，建议客户采用同时上电或 3.3V 先于 1.1V 上电的顺序。



Symbol	Description	Min	Typ	Max	Units
Rt1	3.3V rise time	1	-	100	ms
Rt2	3.3V ready to 1.1V ready time	-5	-	-	ms

3.6 工作电流

WX1860 处理器在不同环境温度下下 4 口千兆全负荷压力测试，测得功耗如下：

环境温度（℃）	电流				功耗 (W)
	VCC11A (mA)	VCCK (mA)	VCCIO (mA)	VCC33A (mA)	
55	429	356	25.6	269	1.8
70	432	382	26.1	278	1.9
85	432	422	26.3	280	2.0

4 SPI Flash 推荐型号

厂家	型号
winbond	W25Q80DV 系列
microchip	SST25VF080B 系列
兆易创新	GD25Q80 系列

5 订购信息

序号	产品型号	分类	产品描述	描述
1	WX1860A2	通用	芯片（0℃-70℃）,40nm,2 口	闪迅 2 端口通用千兆网络控制器芯片
2	WX1860A4	通用	芯片（0℃-70℃）,40nm,4 口	闪迅 4 端口通用千兆网络控制器芯片
3	WX1860AL1	专用	芯片（-40℃-85℃）,40nm,1 口，支持国密 SM2/SM3/SM4	闪迅 1 端口专用千兆网络控制器芯片
4	WX1860AL2	专用	芯片（-40℃-85℃）,40nm,2 口，支持国密 SM2/SM3/SM4	闪迅 2 端口专用千兆网络控制器芯片
5	WX1860AL4	专用	芯片（-40℃-85℃）,40nm,4 口，支持国密 SM2/SM3/SM4	闪迅 4 端口专用千兆网络控制器芯片

说明：1 端口芯片只有 N0 可用，2 端口芯片只有 N0，N1 可用，N2，N3 硬件上已经没有任何功能，可以悬空。四端口芯片 N0，N1，N2，N3 可用。